# Program Overview

A concise description of the design of your program, including a flowchart or other schematic representation.

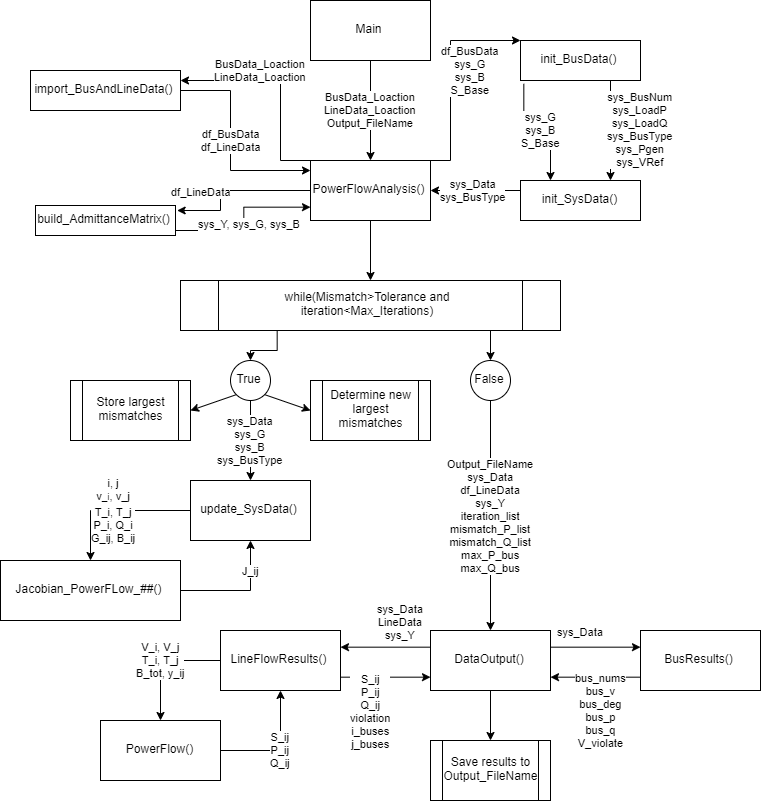


Figure 1: Flow chart of Power Flow Analysis program

# Program Validation

A description of the tests that you performed to verify the correctness of your program.

We might also include any missing features/robustness here

* PowerFlow
  + I calculated the current by hand to verify that the current I got from my code equation matched. After I determined that the current matched, I calculated the power by hand and then checked to see if my code output matched the values I got. I then checked to see if those values matched the sample results that are given for the 3-bus example.
* LineFlowResults
  + After assigning each variable a value, I printed the variable to ensure that its value was what I intended for each iteration of the loop. I then checked the resulting powers that I got for inputting those variables into my PowerFlow functions and compared them to the 3-bus sample results. I also checked the line power violation results to see if they also matched with the results from the 3-bus sample problem. I printed out the results of running the function to ensure that the output was what I expected.
* BusResults
  + Like with the LineFlowResults function, I started by printing each variable to make sure they were the values that I intended them to be. I also checked the list of bus voltage violations to see if they matched the 3-bus sample and changed the input values to make sure the if/else loop worked as intended.
* DataOutput
  + Since I was not very familiar with the subfunctions used in this function, I started by checking the format of the created excel spreadsheet and tried changing different inputs to the subfunctions until I obtained a format that fit what I needed. I then created a new excel file after every data addition to ensure that the data was properly being exported to the file.

# Results

## Base Case

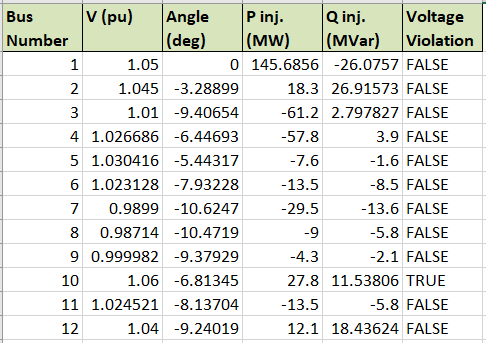


Table 1: Table showing the voltage in per unit, angle in degrees, active power injected in MW, reactive power injected in MVar, and whether the voltage limit was violated at each bus

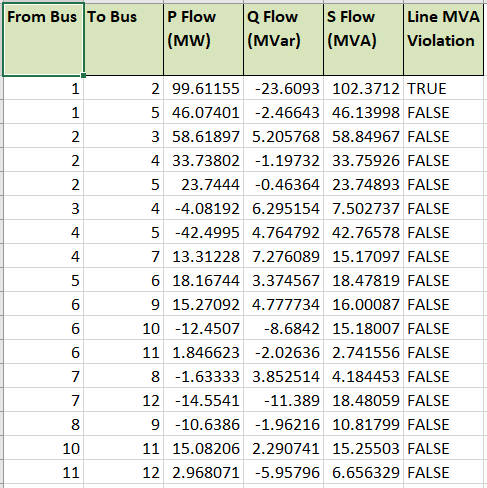


Table 2: Table showing the active, reactive, and apparent power flowing from one bus to another and whether the line MVA limit is violated.

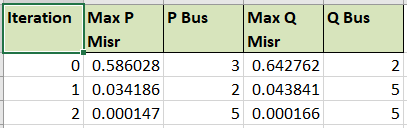


Table 3: Table showing the iterations of convergence with the max active and reactive mismatches and what bus they belong to.

## Contingency 1

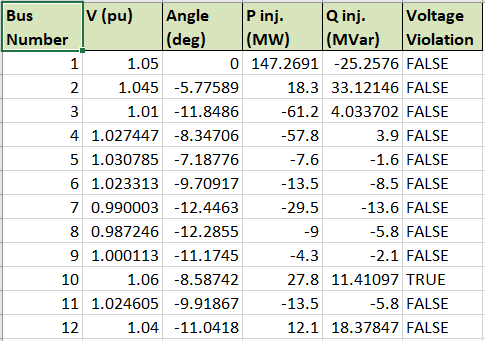


Table 4: Table showing the voltage in per unit, angle in degrees, active power injected in MW, reactive power injected in MVar, and whether the voltage limit was violated at each bus

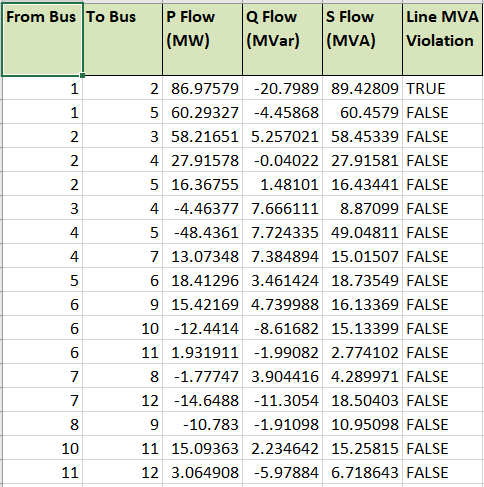


Table 5: Table showing the active, reactive, and apparent power flowing from one bus to another and whether the line MVA limit is violated.

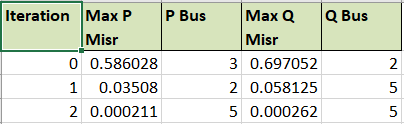


Table 6: Table showing the iterations of convergence with the max active and reactive mismatches and what bus they belong to.

## Contingency 2

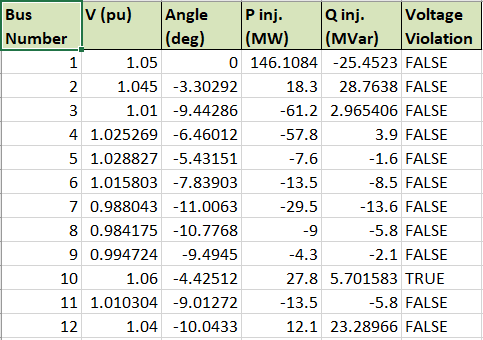


Table 7: Table showing the voltage in per unit, angle in degrees, active power injected in MW, reactive power injected in MVar, and whether the voltage limit was violated at each bus

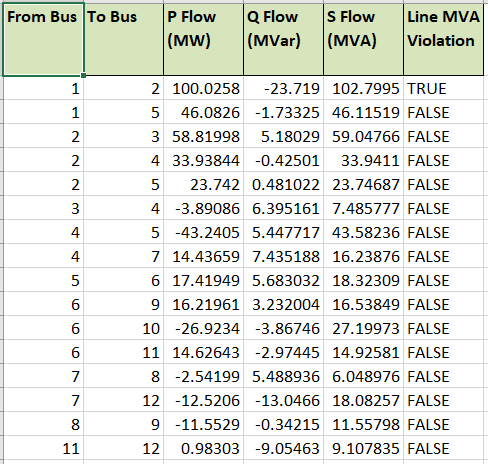


Table 8: Table showing the active, reactive, and apparent power flowing from one bus to another and whether the line MVA limit is violated.

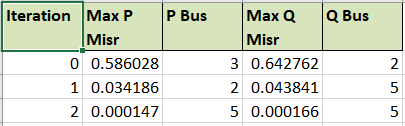


Table 6: Table showing the iterations of convergence with the max active and reactive mismatches and what bus they belong to.

## Discussion of Results

Do they make sense? Why?

# Team Contribution

“I helped”

-Eliot Nichols

# Appendix

<http://www.planetb.ca/projects/syntaxHighlighter/popup.php>